Claims

What is claimed is:

1. A method for implementing deterministic based broken scan chain diagnostics comprising the steps of:

generating a deterministic test pattern;

loading the deterministic test pattern into each scan chain in a device under test using lateral insertion via system data ports and applying system clocks;

unloading each scan chain and identifying a last switching latch in each scan chain;

repeating the generating, loading, and unloading testing steps a selected number of times; and

checking for consistent results; and responsive to consistent results being identified, sending the identified last switching latch to a Physical Failure Analysis system.

2. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 further includes the steps responsive to consistent results not being identified, of selecting another deterministic test pattern; and repeating the testing steps a selected number of times.

3. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system.

4. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using perturbations of one base deterministic test pattern from a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system.

5. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 4 wherein the step of using perturbations of one base deterministic test pattern includes the steps of applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing a selected perturbation matrix entry using said exclusive OR.

6. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 5 includes the steps of providing a perturbation matrix with a plurality of perturbation matrix entries including selected ones of no invert, all invert, a predefined bit invert; rotate, and invert rotate.

7. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using a software Pseudo Random Pattern Generator (PRPG).

8. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using a set of deterministic test patterns resident in a memory.

9. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying deterministic values of the deterministic test pattern to selected one of scan chain inputs and primary inputs.

10. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying perturbation deterministic values of the deterministic test pattern to selected one of scan chain inputs and primary inputs.

11. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying random data from a software Pseudo Random Pattern Generator (PRPG) to scan chain inputs and primary inputs.

12. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying output values from an exclusive OR receiving one base deterministic test pattern from a base deterministic test pattern set and a selected perturbation matrix entry.

13. Apparatus for implementing deterministic based broken scan chain diagnostics comprising:

a set of deterministic test patterns;

a test control program for loading a deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks; unloading each scan chain and identifying a last switching latch in each scan chain; repeating the generating, loading, and unloading testing steps a selected number of times; and checking for consistent results and responsive to consistent results being identified, sending the identified last switching latch to a Physical Failure Analysis system.

14. Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 13 wherein said set of deterministic test patterns includes a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system.

15. Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 13 wherein said set of deterministic test patterns includes perturbations of one base deterministic test pattern from a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system.

16. Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 15 wherein said perturbations of one base deterministic test pattern is generated by applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing a selected perturbation matrix entry using said exclusive OR.

17. Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 16 includes a perturbation matrix having a plurality of perturbation matrix entries including selected ones of no invert, all invert, a predefined bit invert; rotate, and invert rotate.

18. Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 13 wherein said set of deterministic test patterns includes a software Pseudo Random Pattern Generator (PRPG) for generating a deterministic test pattern.

19. A computer program product for implementing deterministic based broken scan chain diagnostics of a device under test in a computer test system, said computer program product including instructions executed by the computer test system to cause the computer system to perform the steps of:

generating a deterministic test pattern;

loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks;

unloading each scan chain and identifying a last switching latch in each scan chain;

repeating the generating, loading, and unloading testing steps a selected number of times; and

checking for consistent results; and responsive to consistent results being identified, sending the identified last switching latch to a Physical Failure Analysis system.

20. A computer program product for implementing deterministic based broken scan chain diagnostics as recited in claim 19 includes the steps responsive to consistent results not being identified, of selecting another deterministic test pattern; and repeating the testing steps a selected number of times.